UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/833,260	04/10/2001	Hans-Jurgen Hacke	GR 00 P 1708	2776

7590 01/15/2004

LERNER AND GREENBERG, P.A.
Post Office Box 2480
Hollywood, FL 33022-2480

EXAMINER	
PAREKH, NITIN	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 01/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/833,260	HACKE, HANS-JURGEN	
	Examiner	Art Unit	
	Nitin Parekh	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *51-56,58-71 and 78-107* is/are pending in the application.

4a) Of the above claim(s) *78-104* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *51-56,58-71 and 105-107* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 April 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Request for Continued Examination

1. A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/30/02 has been entered. An action on the RCE follows.

2. The amendment filed on 09/30/2002 has been entered.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims.

A. The lines 2-6 of the claims 53, 60, 62, 67 and 68 include the limitations "an intermediate carrier having a contact connection area and flat conductors wherein said contact area of the electronic device is configured opposite the contact connection area of the intermediate carrier".

Therefore, the intermediate carrier having a contact connection area and flat conductors and the contact area of the electronic device being oppositely configured must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claim 61 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The claim limitations as recited in claim 61, lines 4-6 include: "said contact element having a length that is at least 5% greater than the largest length difference with regard to said centrally located neutral point of the substrate in event of maximum thermal cycling".

It is not clear from the description in the specification what conditions and parameters are referred to define "maximum thermal cycling" so that a dimensional comparison can be made for the "length of the contact element" and the respective

"length difference/increase" with respect to centrally located neutral point of the substrate.

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claim 61 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claim limitations as recited in claim 61, lines 4-6 include: "said contact element having a length being at least 5% greater than the largest length difference with regard to said centrally located neutral point of the substrate in event of maximum thermal cycling".

It is not clear from the description in the specification what conditions and parameters are referred to define "maximum thermal cycling" so that a dimensional comparison can be made with respect to the length dimension.

Claim R j ctions - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 52-56, 58-71 and 105-107 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yanof et al. (US Pat. 5476818) in view of Khandros et al. (US Pat. 5917707).

A. Regarding claim 52, Yanof et al. disclose an electronic device package (Fig. 1-3) having a contact structure, the device/package comprising:

- a substrate (40/11 in Fig. 3) having top and bottom surfaces (12 and 13 respectively in Fig. 3)
- the substrate comprising conventional electronic circuit interconnects, pads, contacts, ground/signal planes, etc. on the top and bottom surfaces and interconnecting vias (Col. 2, lines 40-60)
- the circuit interconnect including a plurality of contact areas/pads (19 in Fig. 3; Col. 2, line 52)

- the contact area including microscopically small conductive probe/contact element (CP/CE-22/36/35 in Fig. 3) having microscopically small size/dimensions (Col. 5, lines 50-55), and
- the CP/CE having a base (22 in Fig. 3) and a substantially straight part integrally formed at an oblique angle with the base (see 35/36 with respect to 22 in Fig. 3; Col. 5, lines 50-52), the straight part extending from the contact area in three dimensions deviating from orthogonal and parallel directions from the top surface and the electronic circuit interconnect areas/pads and being angularly disposed obliquely relative to the top surface of the substrate in an unstressed condition (Col. 4, lines 25-27; Col. 5, lines 50-52)

(Fig. 3 and 1-7; Col. 2, line 20- Col. 6, line 63).

Yanof et al. fail to teach the contact area being microscopically small.

Khandros et al. an electronic device/package having a contact structure comprising a substrate including microscopically small contact areas and contact elements (103 and 122 in Fig. 2) where the contact areas have small/microscopic dimensions ranging 2-50 mils (Col. 4, line 40).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate microscopically small the contact area as taught by Khandros et al. so that the connection density can be increased in Yanof et al's device.

B. Regarding claim 52, forming or performing the straight part do not distinguish over Yanof et al. and Khandros et al., because only the final product is relevant, not the process of making such as "integrally forming or performing" or "forming by bonding" or "forming by fusion or lamination or hot-pressing" or forming by pre/post deposition". Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marrosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not . Note that applicant has the burden of proof in such cases, as the above case law makes clear. See also MPEP 706.03(e).

Regarding claim 53, Yanof et al. and Khandros et al. teach substantially the entire claimed structure as applied to claim 52 above, wherein Yanof et al. further teach the device being in combination with intermediate carriers/substrates (see 41/47, 84/47, etc. in Fig. 4 and 7 respectively) having a contact connection area and flat conductors (49 in Fig. 4 and 7) where the contact area of the device is configured being opposite to the

connection area of the intermediate carriers/substrates (see Fig. 2 and 7; Col. 2-4 and 8).

Regarding claim 54, Yanof et al. and Khandros et al. teach substantially the entire claimed structure as applied to claim 52 above, except the substrate being selected from a group consisting of a semiconductor chip and a wafer.

Khandros et al. further teach the substrate of the contact structure comprising a variety of substrates/components including a plastic package, ceramic or silicon package having active/passive semiconductor device/electronic chip (103 in Fig. 2) having an integrated circuit on/near the surface of the substrate (Col. 4, lines 13-36).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the substrate being selected from a group consisting of a semiconductor chip and a wafer having an integrated circuit near the surface of the substrate as taught by Khandros et al. so that the desired circuit connection and that among different substrates can be achieved in Khandros et al. and Yanof et al's device.

Regarding claim 55, Yanof et al. and Khandros et al. teach substantially the entire claimed structure as applied to claim 52 above, except the interconnect having ends wherein at least on contact area of each of the plurality of contact areas is configured on a respective one of the ends of the interconnect.

Khandros et al. further teach a plurality of interconnects having ends and each of the contact areas/elements being configured on the respective ends of each of the interconnects (Fig. 6; Col. 8, lines 5-35).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the interconnect having ends wherein at least on contact area of each of the plurality of contact areas is configured on a respective one of the ends of the interconnect as taught by Khandros et al. so that the desired circuit connection and the device integration can be achieved in Khandros et al. and Yanof et al's device.

Regarding claim 56, Yanof et al. and Khandros et al. teach substantially the entire claimed structure as applied to claim 52 above, wherein Yanof et al. further teach the CP/CE being made of elastically deformable material such as gold (35/36 in Fig. 3; Col. 6, lines 25-40).

Regarding claim 58, Yanof et al. and Khandros et al. teach substantially the entire claimed structure as applied to claim 52 above, wherein Yanof et al. teach the CP/CE (see 35/36 in Fig. 3) being prebent at a solid angle that deviates from a direction orthogonal to the top surface of the substrate (Col. 4, lines 25-27; Col. 5, lines 50-52).

Regarding claim 59, Yanof et al. and Khandros et al. teach substantially the entire claimed structure as applied to claim 52 above, except the substrate having a largest bulging area with a bulge protruding from the surface and having a length from the surface such that the length of the contact element is at least 5% greater than that of the bulge of the largest protruding budging area from the surface of the substrate.

Khandros et al. further teach (Fig. 14) the contact element (CE) having a bulge (211 and 219 respectively in Fig. 14) with a largest bulging area such that a length of the CE is greater than the length over which the bulge of the largest protruding budging area protrudes from the top of the substrate.

Furthermore, the determination of parameters such as dimensions (length, width, etc.) of the contact element/lead, contact area/pad (shape, cross-section, etc.) interconnect wiring//trace, number of contact elements/leads, pitch/spacing, etc. and their effect/interaction due to thermal processing, thermal cycling, differences in thermal expansion of various material, etc. in chip packaging and interconnection technology art is a subject of routine experimentation and optimization to achieve the desired contact resistance, surface connection area, and connection flexibility.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to select the substrate having a largest bulging area with a bulge protruding from the surface and having a length from the surface such that the length of the contact element is at least 5% greater than that of the bulge of the largest protruding budging area from the surface of the substrate as taught by Khandros et al. so that the

desired interconnect flexibility related to the length of the contact element, spacing/height between the substrates, etc. and interconnect bonding strength and reliability can be achieved in Khandros et al. and Yanof et al's device.

Regarding claim 60, Yanof et al. and Khandros et al. teach substantially the entire claimed structure as applied to claim 52 above, except:

a) the device being in combination with intermediate carriers/ having a contact connection area and flat conductors where the contact area of the device is configured being opposite to the connection area of the intermediate carriers/substrates, and

b) the CE having a length which is at least 5% greater than a largest distance between the CE and the contact area and the contact connection area of the intermediate carrier.

a) Yanof et al. further teach the device being in combination with intermediate carriers/substrates (see 41/47, 84/47, etc. in Fig. 4 and 7 respectively) having a contact connection area and flat conductors (49 in Fig. 2 and 7) where the contact area of the device is configured being opposite to the connection area of the intermediate carriers/substrates (see Fig. 4 and 7; Col. 2-4 and 8).

b) Khandros et al. further the CE having a length being 5% greater than the largest distance between the contact areas of the device and the intermediate carrier/PCB (see 418 between 416 and 411 in Fig. 25).

Furthermore, the determination of parameters such as dimensions (length, width, etc.) of the contact element/lead, contact area/pad (shape, cross-section, etc.) interconnect wiring//trace, number of contact elements/leads, pitch/spacing, etc. and their effect/interaction due to thermal processing, thermal cycling, differences in thermal expansion of various material, etc. in chip packaging and interconnection technology art is a subject of routine experimentation and optimization to achieve the desired contact resistance, surface connection area, and connection flexibility.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate device being in combination with intermediate carriers/ having a contact connection area and flat conductors where the contact area of the device is configured being opposite to the connection area of the intermediate carrier as taught by Yanof et al. and the CE having a length which is at least 5% greater than a largest distance between the CE and the contact area and the contact connection area of the intermediate carrier as taught by Khandros et al. so that the desired interconnect flexibility related to the length of the contact element, spacing/height between the substrates, etc. and interconnect boding strength and reliability can be achieved in Khandros et al. and Yanof et al's device.

Regarding claim 61, Yanof et al. and Khandros et al. teach substantially the entire claimed structure as applied to claim 52 above, except the contact element having a length being at least 5% greater than the largest length difference with regard to a centrally located neutral point (CNP) of the substrate in an event of maximum thermal cycling.

The determination of parameters such as dimensions (length, width, etc.) of the contact element/lead, contact area/pad (shape, cross-section, etc.) interconnect wiring//trace, number of contact elements/leads, pitch/spacing, etc. and their effect/interaction due to thermal processing, thermal cycling, differences in thermal expansion of various material, etc. in chip packaging and interconnection technology art is a subject of routine experimentation and optimization to achieve the desired contact area, connection flexibility and interconnect strength and reliability.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to select the contact element having a length being at least 5% greater than the largest length difference with regard to a centrally located neutral point (CNP) of the substrate in event of maximum thermal cycling so that the desired interconnect flexibility related to the length of the contact element, spacing/height between the substrates, etc. desired contact resistance/surface connection area and reliability can be achieved in Khandros et al's device.

Regarding claim 62, Yanof et al. and Khandros et al. teach substantially the entire claimed structure as applied to claims 52, 53, 60 and 61.

Regarding claim 63, Yanof et al. and Khandros et al. teach substantially the entire claimed structure as applied to claim 52 above, except the contact area and CE being produced from an identical alloy.

Khandros et al. further teach using the same metal/alloy as gold for the CE and the pad/contact area to achieve low resistance for the contact structure (Col. 16, line 10).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to select the contact area and CE being from an identical alloy as taught by Khandros et al. so that the desired resistance and reliability can be achieved in Khandros et al and Yanof et al's device.

Regarding claims 64 and 65, Yanof et al. and Khandros et al. teach substantially the entire claimed structure as applied to claim 52 above, wherein Yanof et al. further teach the CE being made of gold/gold alloy (36 in Fig. 3; Col. 5, lines 30-40), but Yanof et al. and Khandros et al. fail to teach the contact area being produced from an aluminum and CE being of a copper alloy.

Khandros et al. further teach the contact structure having CE being made of copper (Col. 6, line 66) and the pad/contact area being made of an aluminum metal/alloy (Col. 16, lines 10-15).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to select the CE being made of copper and the contact area being produced from an aluminum alloy as taught by Khandros et al. so that the fabrication and processing can be simplified and the strength of the CE can be improved in Khandros et al and Yanof et al's device.

Regarding claim 66, Yanof et al. and Khandros et al. teach substantially the entire claimed structure as applied to claim 52 above, except the CE being designed as a contact pin.

Yanof et al. further teach external contacts and via interconnects including CE being functional/designed in a variety forms such as an external contact pin, contact tab, bump, etc. (Col.2, lines 48-53).

Khandros et al. teach substantially the entire claimed structure as applied to claim 52 above, and further teach the contact structure being such that the contact element can be designed/configured as a contact pin (106 in Fig. 1) having an end with a contact head (112 in Fig. 1), the end being remote from the contact area (see 112 and 103 in Fig. 1; Col. 6, line 26; Col. 8, line 51).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to select the CE being designed as the contact pin as taught by Khandros et al. so that the external connection capability can be enhanced and the interconnect strength can be improved in Khandros et al and Yanof et al's device.

Regarding claim 67, Yanof et al. and Khandros et al. teach substantially the entire claimed structure as applied to claims 52, 53, 61 and 66 above, except the contact pin having a diameter being not greater than half of the shortest linear dimension of the contact area.

Khandros et al. further teach the contact area having a shortest linear dimension of about 2.0 mils (Col. 4, line 40) and the diameter of the pin being 0.25 mils (Col. 4, line 53) such that the diameter of the pin is no greater than half of the shortest linear dimension of the contact area.

Furthermore, the determination of parameters such as dimensions of the contact element/lead including a diameter/length, contact area/pad, interconnect wiring//trace, number of contact elements/leads, pitch/spacing, etc. and their effect/interaction due to thermal processing, thermal cycling, differences in thermal expansion of various material, etc. in chip packaging and interconnection technology art is a subject of routine experimentation and optimization to achieve the desired contact resistance, surface connection area, connection flexibility and reduced bonding defects.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to select the contact pin having a diameter being not greater than half of the shortest linear dimension of the contact area so that electrical shorting and bonding defects can be prevented in Khandros et al. and Yanof et al 's device.

Regarding claim 68, Yanof et al. and Khandros et al. teach substantially the entire claimed structure as applied to claims 52, 53, 62, 66 and 67 above.

Regarding claims 69-71, Yanof et al. and Khandros et al. teach substantially the entire claimed structure as applied to claims 52, 66 and 68 above, except the contact head being coated with a coating selected from a group consisting of a nickel and gold or a solderable metal alloy or solder respectively.

Khandros et al. further teach using the contact pin having the head being formed with a gold or lead/tin solder coating (Col. 4, lines 46-51).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the contact head being coated with a coating selected from a group consisting of a nickel and gold or a solderable metal alloy as taught by Khandros et al. so that contact resistance can be reduced and the strength of the CE can be improved in Khandros et al. and Yanof et al 's device.

A. Regarding claims 105 and 106, Yanof et al. and Khandros et al. teach substantially the entire claimed structure as applied to claim 52 above, except the CE being configured as a contact pin having a diameter which is no greater than half of a shortest linear dimension of the contact area.

Khandros et al. further teach:

- the contact structure being such that the CE can be designed/configured as a contact pin or pin-shaped configuration having a base and an extended part having a predetermined diameter (107/106 in Fig. 1; Col. 4, line 54), and
- the contact area having a shortest linear dimension of about 2.0 mils (Col. 4, line 40) and the diameter of the pin being 0.25 mils (Col. 4, line 53) such that the diameter of the pin is no greater than half of the shortest linear dimension of the contact area.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the CE being configured as a contact pin with the extended part comprising a pin-shaped configuration, the pin having a diameter which is no greater than half of a shortest linear dimension of the contact area as taught by Khandros et al. so that the desired contact resistance can be achieved, electrical

shorting can be prevented and reliability of the interconnection can be improved in Khandros et al. and Yanof et al 's device.

B. Regarding claim 105, forming or performing the straight part do not distinguish over Yanof et al. and Khandros et al., because only the final product is relevant, not the process of making such as "integrally forming or performing" or "forming by bonding" or "forming by fusion or lamination or hot-pressing" or forming by pre/post deposition". Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marrosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not . Note that applicant has the burden of proof in such cases, as the above case law makes clear. See also MPEP 706.03(e).

Regarding claim 107, Yanof et al. and Khandros et al. teach substantially the entire claimed structure as applied to claim 105 above, except the part extending from the base has a free end opposite the base and is configured for detachably receiving a test head.

Khandros et al. teach the extended part of the pin contact being adapted for a variety of flexible, resilient and detachably receivable/removable configurations for test and burn-in applications (Fig. 1-38; Col. 4-23).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the part extending from the base has a free end opposite the base and is configured for detachably receiving a test head as taught by Khandros et al. so that the connection flexibility can be improved and the desired test/repair requirements can be achieved in Khandros et al. and Yanof et al 's device.

Response to Arguments

A. Regarding claim 61, applicant contends that one of ordinary skill in the art would understand the conditions of "maximum thermal cycling".

However, the thermal cycling (TC) as described on page 8, line 13-page 9, line 3, does not describe what parameters are used to perform the maximum thermal cycling. TC process involves a number of parameters such as temperature, time, ramp rate, cycle/frequency, etc., each having respective operating range. Without clear description of operating conditions of such parameters, the difference (increase/decrease) in the

length dimension of the contact element with respect to the CNP of the substrate as recited in claim 61 cannot be compared or evaluated.

B. Applicant's arguments with respect to claims 52-56, 58-60, 62-71 and 105-107 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 703-305-3410. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 703-305-1690. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Nitin Parekh

NP

01-09-04

NITIN PAREKH
PATENT EXAMINER
TECHNOLOGY CENTER 2800